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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,964	01/10/2002	Frederic Reblewski	21044.P002	6410

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EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/06/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,964	REBLEWSKI ET AL.	
	Examiner	Art Unit	
	Sun J Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/10/2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January, 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to application 10/043,964 filed on 01/10/2002. Claims 1 – 24 remain pending in the application.

Drawing Objections

2. Drawing is objected to because of following informalities:

Figures 1 – 3 should respectively be labeled as a **—PRIOR ART—**.

Appropriate correction is required.

Specification Objections

3. Specification is objected to because of the following informalities:

Page 10, line 1, change "temporary create" to **—create temporary—**.

Appropriate correction is required.

Claim Objections

4. Claims are objected to because of the following informalities:

Claim 1, line 4, after "each" insert **—chain—**.
Claim 5, line 1, after "plurality" insert **—of—**.
Claim 5, line 2, change "logic" insert **—logics—**.
Claim 22, line 4, change "comprisees" insert **—comprises—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1 – 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to ***Sample et al.*** in view of U.S. Patent No. 5,644, 496 to ***Agrawal et al.***

7. As to Claim 1, ***Sample et al.*** shows in Fig. 13D structure of a partial ***hybrid multiplexer-crosspoint crossbar*** (i.e., called ***crossbar device*** hereinafter) portion, which comprises a *crosspoint-type crossbar 650* and the *fully encoded multiplexer-type crossbar 630* – [Fig. 13D; col. 12, line 61 – col. 13, line 20].

The *partial cross device portion* shown in Fig. 13D contains eight (8) ***inputs lines 611*** and one (1) ***output line***. A *complete* crossbar device contains a plurality of *partial crossbar device portions*. Therefore, it is inherent that the complete crossbar device can be designed to have a *multiple number of input lines* (e.g., ***n input lines***) and *a multiple number of output lines* (e.g., ***m output lines***).

Sample et al. do not teach a method of placing a ***pass transistor*** at the input of each *input line* for use in selectively coupling the *input line* to the output of the crossbar device. But, Agrawal et al. teach this method.

Agrawal et al. show in Fig. 6A inserting a ***PIP 521***, which contains a ***pass transistor 35*** as depicted in Fig. 2A, on the ***line 503*** connecting to one of the input lines of *UPM 501* (i.e., User Programmable Multiplexer), which is a ***multiplexer-type crossbar device***. It is inherent that the ***pass transistor 35*** can be used to selectively couple the signal on ***line 503*** to the output of ***UMP501*** (crossbar device) thereby gain more control over the signal flow and prevent glitch getting into UMP501 when it is not ready for operation.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of Agrawal and Sample et al. by inserting a *pass transistor* (*PIP 521* of Agrawal et al.) at the input of each input line and with *pass transistor 651* (Fig. 13D of Sample et al.) to constitute a pass transistor chain thereby prevent glitches getting the crossbar device, when it is not ready for operation and gaining more control over the signal flow for selectively coupling the n input lines to the m output lines of the crossbar device.

For reference purpose, the explanations given above in response to Claim 1 are call **[Response A]** hereinafter.

8. As to Claim 2 and 3, as explained in **[Response A]** given above, a *pass transistor* (i.e., ***pass transistor 35*** in ***PIP 521***) [Fig. 6A and Fig. 2A of *Agrawal et al.*] is to be placed at input port of each *input line 611* [Fig. 13D of Sample et al.]. Referring to Fig. 13D of Sample et al., when all ***pass transistors 35*** are inserted, each of the plurality of chains of pass transistor consists of two pass transistors: ***pass transistor 35*** to be inserted at a *input line 611* is a ***first pass transistor***; ***pass transistor 651*** in *unit 650*, which is connected to a *output line* 620, is a ***second pass transistor***.

For reference purpose, the explanations given above in response to Claims 2 and 3 are call **[Response B]** hereinafter.

9. As to Claim 4, as explained in **[Response A]** given above, a ***pass transistor 35*** is to be inserted at each ***input line*** (i.e., ***input side of each chain***). As illustrated in Fig. 2A of Agrawal et al., each ***pass transistor 35*** is coupled to a ***MEM CELL 36*** (i.e., memory element), which is used to control the input signal to each chain. Therefore, there is a plurality of memory elements (***MEM CELLs 36***) coupled to a plurality of input lines of the crossbar device.

For reference purpose, the explanations given above in response to Claim 4 are call **[Response C]** hereinafter.

10. As to Claim 5, Sample et al. show in Fig. 13D and teach using a **2-to-4 *DECODER 640*** (i.e., ***p-to-q decoder logic***; where p = 2, q = 4) for coupling the input lines of a ***crossbar unit 630*** to control outputting one of input signals to ***crossbar output 620***. As explained in **[Response A]** given above, the complete crossbar device should consist of a plurality of ***crossbar units 630***. Therefore, it is inherent that the complete crossbar device has a plurality of ***2-to-4 DECODERs 640***.

For reference purpose, the explanations given above in response to Claim 5 are call **[Response D]** hereinafter.

11. As to Claim 6, reasons are included in **[Response C]** given above.

12. Claims 7, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to Sample et al. in view of applicants' admitted prior art and U.S. Patent No. 6,175,952 to Patel et al.

13. As to Claim 7, Sample et al. show in Fig. 13D a crossbar device. It is inherent that a cross connect system can have a plurality of crossbar devices, and one crossbar device can electrically couple to another crossbar device. Sample et al. do not teach a method of installing an *output buffer* at each output line of a crossbar device. But applicants' admitted prior art shows this method in Figs. 1a, 2 and 3.

It is a basic concept and also is a ***digital data-transmission standard*** that an ***output buffer*** should be installed at the output port of each digital data device (e.g., crossbar device) to adjust its output signal to an acceptable higher level before feeding into another digital data device (e.g., crossbar device) in order to maintain a high quality of digital data.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of applicants' admitted prior art to install an output buffer at each output line of a crossbar device to adjust the output signal to an acceptable higher level before coupling to another crossbar device in order to maintain a high quality of digital data.

Referring to Fig. 13D of Sample et al., when an output buffer is in installed at the ***crossbar output 620***, it is inherent that the output buffer is electrically associated with the ***memory element 652***, which control the electrical signal passing through the ***pass transistor 651***.

Sample et al. also do not teach ***voltage supply structure*** as recited in the claim. However, ***Patel et al.*** teach this subject matter in Fig. 23 [col. 25, line 56 – col. 26, line 26; col. 26, line 43 – 55]. Notice that the ***cross-coupled latch 2310*** in Fig. 23 is an ***output buffer*** and its voltage at a VCC1 (e.g., Vdd) level. Patel et al. show in Fig. 23 and teach ***voltage supply arrangement*** that the ***isolation device 2315*** contains a ***pass-transistor 2320*** [col. 26, line 43 – 55], and its supply voltage VCC2 can be coupled from an ***internal circuitry*** of the integrated circuit [col. 24, line 63 – 64]. Patel et al. teach that, in order to achieve a desired VCC (i.e., Vdd) level at the output, the bias supply voltage of a pass-transistor should be about VCC + $|Vth|$, where $|Vth|$ is a threshold voltage of pass-transistor [col. 13, line 61 – 63; col. 13, line 36 – 44].

Patel et al. show and teach the voltage supply arrangement in Fig. 23, which has similar components (i.e., pass-transistor 651 and output buffer) as that disclosed by Sample et al. (Fig. 13D) and applicant's admitted prior art (Fig. 2).

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Patel et al. on *voltage supply arrangement* in order to maintain the input voltage of the output buffers at a desired VCC (i.e., Vdd) level.

For reference purpose, the explanations given above in response to Claim 7 are call **[Response E]** hereinafter.

14. As to Claims 13 and 14, Sample et al. teach that the crossbar device is an integrated circuit device – [abstract]. Patel et al. teach that the *voltage supply arrangement* (i.e., voltage supply structure) is designed in an integrated circuit – [abstract]. Therefore, reconfigurable circuit (i.e., crossbar device + voltage supply structure) can be implemented as a stand-alone integrated circuit design or a building

block (i.e., block of an integrated circuit) being integrated with other devices to provide data cross-connect functions.

For reference purpose, the explanations given above in response to Claims 13 and 14 are call **[Response F]** hereinafter.

15. Claims 8 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to Sample et al., applicants' admitted prior art and U.S. Patent No. 6,175,952 to Patel et al. in view of U.S. Patent No. 5,644, 496 to Agrawal et al.

16. As to Claims 8 – 12, Sample, applicants' admitted prior art and Patel et al. (call Sample_App_Patel et al. hereinafter) teach all the subject matter in Claim 7. Sample_App_Patel et al. do not teach a method of inserting a pass-transistor and control memory element at each input line. But Agrawal et al. teach this method. Reasons are listed below:

- Reasons for Claim 8 are included in **[Response A]** given above.
- Reasons for Claims 9 and 10 are included in **[Response B]** given above.
- Reasons for Claim 11 are included in **[Response A]** and **[Response E]** given above.
- Reasons for Claim 12 are included in **[Response C]** given above.

17. Claims 15, 16, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to Sample et al. and applicants' admitted prior art in view of U.S. Patent No. 5,744,990 to Burstein et al.

18. As to Claim 15, Sample et al. show in Fig. 13D a crossbar device and applicants' admitted prior art (Fig. 3) shows and teaches installing an output buffer at each output line as explained in **[Response E]** above. But Sample et al. and applicant's admitted prior art (called ***Sample_App et al.*** hereinafter) do not teach a method of comprising a power-on circuitry in the configurable circuit, which is coupled to the crossbar devices to force the output buffers to a known state at power-on. But Burstein et al. teach this method.

Burstein et al. show a ***power-on reset*** (***POR***) ***generating circuitry*** in Fig. 1. Burstein et al. teach that digital design require some type of ***POR*** signal during initial turn-on to *initialize various components in the system*, such as *flip-flops*, memory devices (e.g., input/output buffers) etc. – [col. 1, line 13 – 18]. Therefore, it is inherent that ***POR signal*** is used to initialize each digital circuit to a known state, which is safe for operation. It is well known in the art that the ***POR circuit*** is a ***standard built-in unit*** in any memory-related digital equipment (e.g., crossbar device). Burstein et al. teach using ***POR signal*** to reset a ***flip-flop*** thereby to "zero" a *memory device* (e.g., output buffer) at power-on – [col. 1, line 13 – 18].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have used the teachings of Burstein et al. to include a ***POR circuitry*** in the reconfigurable, which is coupled to the crossbar devices to force the output buffers to a *known safe state* at power-on.

For reference purpose, the explanations given above in response to Claim 15 are call **[Response G]** hereinafter.

19. As to Claim 16, Burstein et al. teach using ***POR signal*** to reset a ***flip-flop*** thereby to "zero" a *memory device* (e.g., output buffer) at power-on – [col. 1, line 13 – 18].

20. As to Claims 23 and 24, reasons are included in **[Response F]** given above.

21. Claims 17 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to Sample et al., applicants' admitted prior art and U.S. Patent No. 5,744,990 to Burstein et al. in view of U.S. Patent No. 5,644, 496 to Agrawal et al.

22. As to Claim 17 – 21, Sample, applicants' admitted prior art and Burstein et al. (called ***Sample_App_Burstein et al.*** hereinafter) teach all the subject matters on crossbar except a method of inserting a pass-transistor at the input port of each input line. But Agrawal et al. teach this method. Reasons are listed below:

- Reasons for Claim 17 are included in **[Response A]** given above.
- Reasons for Claims 18 and 19 are included in **[Response B]** given above.
- Reasons for Claim 20 are included in **[Response A]** and **[Response E]** given above.
- Reasons for Claim 21 are included in **[Response C]** given above.

23. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,289, 494 to Sample et al., applicants' admitted prior art, U.S. Patent No. 5,744,990 to Burstein et al. in view of U.S. Patent No. 6,175,952 to Patel et al.

24. As to Claim 22, ***Sample_App_Burstein et al.*** teach all the subject matters except the method of voltage supply structure. But Patel et al. teach this method. Detailed explanations are included in **[Response E]** given above.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (703) 308-4916. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
October 25, 2002

MATTHEW SMITH
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